REMARKS

Claims 1-20 are all the claims presently pending in the application. Claim 20 has been added to help clarify the invention to the Examiner and is based on the description at line 19 of page 12 through line 4 of page 13.

It is noted that Applicants specifically state that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

The Examiner objects to the specification for failing to list the co-pending applications beginning on page 1. Applicants believe the above specification amendment appropriately addresses this concern and respectfully requests that the Examiner reconsider and withdraw this rejection.

The Examiner also objects to the drawings initially filed on September 29, 2003, and to the subsequent replacement drawings filed on December 30, 2003. Since the replacement drawings would appear to be in complete compliance with normal patent application drawings and the Examiner fails to identify a specific problem, Applicants are unable at this time to address this objection further at this time. Therefore, Applicants respectfully requests that the Examiner clarify in the next Office Action the specific problem for these replacement drawings filed on December 30, 2003.

Claims 1-19 stand rejected under 35 U.S.C. § 101 as allegedly directed to non-statutory subject matter. Claims 1, 2, and 17 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 5,438,669 to Nakazawa et al. Claims 3-16, 18, and 19 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Nakazawa, further in view of Dongarra, et al., "A Set of Level 3 Basic Linear Algebra Subprograms.".

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a software method of improving at least one of efficiency and speed in executing a linear algebra subroutines on a computer having a floating point unit (FPU) capable of overlapping loading data and processing of the data. A load instructions are used to preload data in a timely manner into floating point registers (FRegs) of the FPU from the L1 cache from an execution code controlling operation of the FPU that is performing the linear algebra subroutines in a near optimal way.

In a programming language, this can be done by "unrolling", which preloads data in advance into the FRegs and then executes corresponding FReg instructions of the linear algebra subroutine.

As explained beginning at line 17 of page 3 of the specification, a number of advancements have been made in the computerized processing of linear algebra routines on computers of various architectures.

The claimed invention addresses one of the problems identified by the present inventors given a specific interface with a recent floating point unit (FPUs) design that typically is used for such linear algebra routine processing.

II. THE 35 USC §101 REJECTION

Claims 1-17 stand rejected under 35 U.S.C. §101. The rejection states:

"*Claims 1 and 17 are directed to computer implemented methods for performing execution of a linear algebra subroutine which can be interpreted as a method of calculation that the inputs are numbers and the results are also numbers. Claim 17 further claims providing service for solving and applying a scientific/engineering problem, which is only an abstract idea. In order for a computer related invention to be statutory, the claimed invention must accomplish a practical application. That is, the claimed invention must transform an article or physical object to a different state or thing, or produce a useful concrete and tangible result. That results of the invention are merely numerical values without practical application recited in the claims and thus is not useful, concrete and tangible. Therefore, the claimed inventions are directed to non-statutory subject matter as the claims fail to assert a practical application to the invention.*

It should be noted that claim 17 defines a "signal-bearing medium" that could be any type of "digital and analog and communication links and wireless", which the applicant has indicated as being included in the scope of "a signal-bearing medium". (Page 17, lines 15-16, "or other suitable signal-bearing media including transmission media such as digital and analog and communication links and wireless"). Because "signal-bearing medium" can be interpreted as a signal encoded with functional descriptive material, which does not fall within any of the categories of patentable subject matter set forth in 35 U.S.C. §101."

In response, Applicants first respectfully submit the understanding of the Examiner seems somewhat confused on statutory subject matter. First, Applicants submit that the "useful, tangible and concrete result" test applies only for those inventions where there is a legitimate issue whether the claimed invention is directed toward one of the judicial exceptions (e.g., an abstract idea, a law of nature, or natural phenomena).

In the instant application, the claimed invention of the method claims 1-5 is clearly directed toward improving efficiency and speed on a computer performing a linear algebra routine and is not directed toward claiming a mathematical algorithm in the abstract, as was arguably true in the Supreme Court holding in *Benson*, 409 U.S. 63 (1972). Therefore, these claims are not even within one of the judicial exceptions that require the "useful, tangible and concrete" analysis of *State Street* and *AT&T*.

Nor is the present invention pre-empting any of the linear algebra subroutines or routines, since these subroutines/routines can still be executed at the slower, less efficient manner.

Moreover, Applicants submit that the result of improving efficiency and speed in computer processing in the manner described by the present invention inherently satisfies the requirement for providing a result that is useful, concrete, and tangible.

Therefore, claims 1-5 are clearly directed toward statutory subject matter. It is further noted that the "useful, tangible and concrete" test is applied to the claimed invention as a whole and does not require that an arbitrary result be articulated in the independent claim, as

the Examiner implies.

Relative to claims 6-11, these claims are clearly directed to an apparatus (e.g., a "machine") and clearly falls in one of the four categories specifically identified in 35 U.S.C. § 101 and are, therefore, directed toward statutory subject matter.

Claims 12-16 are directed to a "signal-bearing medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus", not to a "signal-bearing medium" in isolation. Applicants submit that the additional wording clearly are directed to a process defined to be executed on a computer and, therefore, clearly qualifies as one of the four categories listed in 35 U.S.C. §101. However, in an effort to expedite prosecution, Applicants have changed "signal-bearing" to "computer-readable." Therefore, the Examiner is respectfully requested to reconsider and withdraw this rejection for claims 12-16.

Relative to claims 17-19, Applicants respectfully submit that providing consultation services would not be an abstract idea, since these claims relate to a "consultation service" based on using the present invention.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE PRIOR ART REJECTIONS

The Examiner alleges that Nakazawa teaches the present invention described by claims 1, 2, and 17, and, when modified by Dongarra, renders obvious claims 3-16, 18, and 19. Applicants submit, however, that there are elements of the claimed invention which are neither taught nor suggested by Nakazawa.

As explained in the second sentence (e.g., in column 1 at lines 12-17), Nakazawa addresses a processing method in a computer architecture in which a cache is not so effective.

In this architecture, a large number of data registers accessible to main memory are used. To overcome this design deficiency, Nakazawa introduces preloading of data from main memory directly into these data registers.

In contrast, in the present invention, the L1 cache is used for the matrix data transfer between main memory and the FPUs, so that Nakazawa clearly teaches against the approach of the present invention. That is, the present invention clearly addresses the data preloading into the FPUs using the cache and does so using a software mechanism that does not require the hardware registers of the Nakazawa computer architecture.

Secondary reference Dongarra fails to overcome this basic deficiency of Nakazawa.

In summary, the method in Nakazawa provides a hardware solution to get matrix data from memory to the processor and will work only for the 1995 hardware described therein. In contrast, the present invention provides a general software solution for matrix multiplication, possibly in combination with one or more of the six other co-pending applications.

Therefore, Nakazawa teaches clearly that matrix data using his processing unit cannot be efficiently retrieved from memory using typical cache architecture. In contrast, the present invention provides basic ground rules for preloading in the context of matrix multiplication kernels. This is novel and not obvious from Nakazawa. That is, relative to independent claim 1 (as well as remaining independent claims), Nakazawa would work only on the now-obsolete 1995 hardware, whereas the present invention is much faster and works with standard cache-based machines.

Hence, turning to the clear language of the claims, in Nakazawa there is no teaching or suggestion of: "A software method of improving at least one of efficiency and speed in executing a linear algebra subroutine in a computer having a floating point unit (FPU) capable of overlapping loading data and processing of said data, said method comprising: for

an execution code controlling operation of said FPU performing said linear algebra subroutine execution, overlapping by preloading data into a floating point register (FReg) of said FPU, said overlapping causing data to arrive into said FReg to be timely executed by FPU operations of said linear algebra subroutine on said FPU", as required by independent claim 1. The remaining independent claims have similar language.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggested by Nakazawa. Therefore, the Examiner is respectfully requested to withdraw this rejection for claims 1, 2, and 17.

Claims 2-16, 18, and 19 stand rejected as unpatentable over Nakazawa, further in view of Dongarra. However, regardless of the propriety of combining Dongarra with Nakazawa, this secondary reference does not overcome the basic deficiency identified above for Nakazawa.

Moreover, the following comments relate to the non-obviousness of additional dependent claims over the prior art of record. Relative to claim 4, Applicants respectfully point out that use of L1 BLAS and what followed, L2 BLAS, do not work efficiently on today's cache-based architecture. The reason is that they are very slow methods.

Relative to claim 5, Nakazawa and, particularly Dongarra, do not use level L3 routines for factorization *per se*, and their methods there are very slow compared to those used in the present invention and the six co-pending applications. It was not obvious to Dongarra to use fast methods for factorization *per se*.

Relative to claim 18, Dongarra does not disclose any detail on how to implement fast BLAS. Dongarra is actually asking computer manufacturers to implement his methods, rather than disclosing fast methods to do this.

Finally, relative to secondary reference Dongarra, Applicants are not attempting to patent matrix multiplication *per se*. Level 3 BLAS are an industry standard for matrix

multiplication. Cayley defined matrix multiplication in 1854 for the first time. Dongarra merely repeats that definition in very slow implementation of matrix multiplication.

Therefore, Applicants submit that all claims are clearly patentable over Nakazawa, even if combined by Dongarra, and respectfully request the Examiner to reconsider and withdraw these rejections.

IV. FORMAL MATTERS AND CONCLUSION

The disclosure has been revised to update the co-pending application data beginning on page 1.

In view of the foregoing, Applicant submits that claims 1-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

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